Design and Analysis of Carbon Nanotube Based Analog Building Blocks and its Applications

SHORT SYNOPSIS

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Certificate

I hereby declare that the short synopsis "**Design and Analysis of Carbon Nanotube Based Analog Building Blocks and its Applications**" being submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy in Electronics & Communication Engineering under faculty of engineering and technology of Manav Rachna International Institute of Research & Studies, Faridabad during the academic year 2022 – 2023. It is a bona fide record of original work carried out under the supervision of **Dr. Vimlesh Singh** and co supervision of **Dr. Laxya** has not been submitted in full or part to any other university or institute for degree or diploma. Further, it is certified that short synopsis is plagiarism free and proof has been submitted.

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ABSTRACT

Analog VLSI is presently playing an essential role in technology. These days, a wide variety of circuits (including amplifiers, filters, comparators, multipliers, oscillators, PLLs, voltage/current references, sample-and-hold circuits, A/D and D/A converters, and high-speed IO interfaces) are being introduced for new information processing applications, such as speech recognition, integrated sensors, handwriting recognition, image processing, etc.

A recently developed material and its associated electronic device/transistor with a strong potential to successfully replace Si and the conventional MOSFET technology is the carbon nanotube (CNT) and a transistor realized by it, that is, the carbon nanotube field effect transistor (CNTFET). CNTs are multiwall and single wall materials with distinct electrical, mechanical, and optoelectronic characteristics. Sumio Lijima of Japan is credited with discovering the first multi-walled carbon nanotubes in 1991, and he and Donald Bethune independently discovered the single wall CNT in 1993. CNTs are graphite sheets that have been rolled into cylindrical shapes and have diameters between 1 and 50 nm and a length of a few micrometers. Because of their enormous aspect ratio, they have special electrical, mechanical, thermal, chemical, and optical capabilities. Their tensile strength is 100 times greater than that of steel, and their thermal conductivity is higher than diamond. Based on their chirality or chirality vector, CNTs have the unique ability to exhibit metallic and semiconducting properties. An important application of CNTs is the realization of CNTFET.

This work is based on a new category of waveform generators which would be design and analyze by H-spice simulation platform. For design of proposed research work analog building blocks of CNTFET will be used for achieving channel lengths optimization of CNTFET at low voltages application. Behavioral properties of designed analog building block will be verified by foundry certified simulation tools.

Keywords – Carbon Nanotubes (CNT), Carbon Nanotube Field Effect Transistor (CNTFET), Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

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1. INTRODUCTION

Information is typically processed in either analog or digital form by electronic systems. Analog and digital circuits have been developed to process the two types of signals. Until around 1960, almost all technology was analog, but digital technology has advanced significantly since the invention of integrated circuits.

Analog systems converted the voltage or current signal proportional to the quantity in which the signal can measurable. In case of continuous state system, any value of voltage/ current can be taken for representing its minimum and maximum value with in the system range.

Similar to analog system different from of digital systems to represent the discrete-state in which one state to represent either voltage/current. Where as in case of linear circuit one variable (voltage or current) is directly proportionate to another variable. Analog circuits mostly use these types of circuits. The fundamental components of linear systems employing analog technology are linear active circuits, sometimes referred to as amplifiers.

1.1 Analog Building Block

When describing and analysis of extremely complicated electric systems, it is often beneficial to think of huge systems as being created from smaller parts known as building blocks. These are the components that may be connected to one other to create bigger circuits or systems. The basic terminal features of the building components, more crucially, appropriately characterize them. Thus, from the standpoint of building blocks, one is only interested in how the blocks perform from the outside.

Advancements in technology have led to the growing popularity of analog building blocks, which in turn has stimulated the development of new building blocks. The Operational Amplifier (OP-AMP) is the one of many of these blocks. There are various types of operational amplifiers, such as the Operational Feedback Amplifier (OFA), the Operational Transconductance Amplifier (OTA), and the Operational Transresistance Amplifier (OTRA), among others. Additionally, current conveyors are categorized into different generations, including the First-Generation Current Conveyor (CCl), Second Generation Current Conveyor (CC-ll), Third Generation Current Conveyor (CC-lll), Dual Output Current Conveyor First Generation (DO-CCl), Dual Output Current Conveyor Second Generation (DO-CCll), and Dual Output Current Conveyor Third Generation (DO-CClll). The Voltage Differencing Transconductance Amplifier (VDTA) and the Current Differencing Transconductance Amplifier (CDTA) are both critical active

components. Nuller-floating mirror elements are used to represent Balanced Output Current Conveyor Second Generation (BO-CCll), Dual Output Inverting Current Conveyor Second Generation (DOl-CCll), Differential Current Conveyor Second Generation (DC-Cll), and Fully Differential Current Conveyor Second Generation (FD-CCll)

1.1.1 Current Conveyors

In both current and mixed mode applications, the current conveyor serves as the essential building element at high frequency usage. Due to limited GBP of operational amplifier. In 1968, Smith and Sedra, presented first generation of current conveyor. Later G-2 & G-3 generation of Current Conveyor were published in 1970 & 1995.

1.1.2 Voltage Differencing Transconductance Amplifier

It is active element of analog building block consist of current source which controlled by voltage difference of two input signal. In VDTA multiple outputs are tuned by transconductance gain. In a voltage differencing transconductance amplifier, the current at the terminal Z is affected by one transconductance gain caused by the differential input voltage between the P (VP) and N (VN) terminals, and the current at the terminals X+ and X- is affected by another transconductance gain caused by the voltage at Z. The external bias current has the ability to electronically control both transconductance gains. When compared to other active blocks, the Voltage Differencing Transconductance Amplifier has the advantage of having two different values of transconductance, allowing multiple applications to be realized with a single active block, including oscillator, biquad filters etc. with one or two capacitors. Another significant aspect of this block is its ability to be employed in a transconductance mode application because voltage is at the input terminals and current is at the output terminals.

1.1.3 Operational Transconductance Amplifier

Operational transconductance amplifiers are among the most significant and useful active devices utilized in the effectively realizing analog integrated circuits. In comparison to an operational amplifier, operational transconductance amplifiers have advantages such as wider bandwidth, larger dynamic range, no excess phase issues, and can be used very effectively in many applications, particularly those with capacitive loads. Furthermore, the presence of an external bias current (Ibias) in an operational

transconductance amplifier increases its flexibility and tunability, which is the most significant advantage of an operational transconductance amplifier.

1.1.4 Operational Transresistance Amplifier

The Operational Transresistance Amplifier is an analog building block with a high gain and a current input voltage output. The input terminals of the Operational Transresistance Amplifier are internally grounded, removing response limitations caused by parasitic capacitances and resistances, making it a good choice for high frequency applications, and the port characteristics are given by (1), where Rm is the transresistance gain of the Operational Transresistance Amplifier.

$$\begin{bmatrix} V_p \\ V_n \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_O \end{bmatrix}. \qquad (1)$$

The Operational Transresistance Amplifier approaches infinity for ideal operation and forces the input currents to be equal. As a result, the operational transresistance amplifier must be used in a negative feedback mode.

1.1.5 Current Differencing Buffered Amplifier

Acar and Ozoguz invented the Current Differencing Buffered Amplifier. The Current Differencing Buffered Amplifier has four terminals: p, n, w, and z, with p and n representing positive and negative input terminals, z representing the current output terminal, and w representing the voltage output terminal.

Because of the low input impedance terminal, Current Differencing Buffered Amplifier is free of parasitic capacitances and thus appropriate for use at high frequency operations. It has the ability to function in both voltage and current modes. giving designers more options. It features a high slew rate and additional options for simplifying the circuit.

1.2 Carbon Nanotube

Design of complex electronic circuits in integrated circuit need to identify the solution in nanomaterials. Nano materials have great adaptability to interface with flexible electronic system. This demands to design of analog building blocks using the cabon nano tube structure. The great extent of functionality of integrated system creates opportunity to explore the Carbon Nanotube structure.

Prior to 1991, there were only two recognized primary allotropes of carbon. Carbon Nanotube was developed in 1991 by Japanese physicist Sumio Lizima.

Nanotubes, a kind of fullerene, are composed of molecular-scale carbon tubes that are stacked in layers like those found in graphite. Each carbon atom in a carbon nanotube is linked by three other carbon atoms through powerful covalent bonds, giving them a very high melting point. A sea of delocalized electrons forms inside the tube as a result, allowing each carbon atom to have an extra electron, which makes nanotubes electrically conductible.

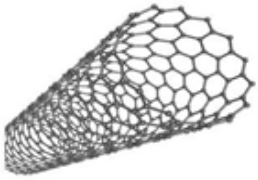
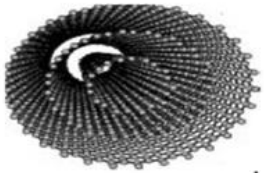
Two-dimensional graphite is folded or rolled into a cylindrical shape to create nanotubes. The interior of a nanotube is hollow. The nanotube is 1-3 nanometers in diameter. The length of a carbon nanotube is far greater than its diameter. Nanotubes are typically a few micrometers long. Carbon nanotubes are two-dimensional graphene sheets that have been folded. Now days the role of Carbon nanotube is more crucial in designing of Very Large-Scale Integration circuits. Carbon Nanotube has many applications in designing of bullet proof jackets for military uses. Carbon Nanotube can combine with other materials to create sports apparels. To create bodies of space ships and air crafts Carbon nanotube is one of the excellent material due to its exceedingly light weight. In VLSI designing Carbon nanotube are one of the best employed materials to create high performance nanoscale thin film transistors that can replace Silicon based transistor in future. This futuristic material is also beneficial to create bio sensors and electro chemical sensors and electrodes (Anode & Cathode) due to their superior electrical properties.

There are different properties of Carbon nanotube that can increase its use in present day circuit designing. The stiffness of Carbon Nanotube is good that make it as rigid as diamond. It has very less gravitational mass and its density is ¼ that of steel, that make it 10 times stronger than steel. Carbon Nanotube has good elastic property and they are good conductor of heat. Its structural shape increases its electrical conductivity. The hexagon shape makes it crystalline structure of

carbon. Three additional carbon atoms form covalent connections to encircle each carbon atom in Carbon Nanotube.

1.2.1 Types of Carbon Nanotubes

Table1: Types of Carbon Nanotubes (Gupta, Gupta and Sharma, 2019.)

Type	Single – Wall	Double - Wall	Multi - Wall
Figure			
Description	A 1-d structure makes up the single-walled carbon nanotubes. Wrapping a layer of atomic single layer graphite termed graphene into a seamless cylinder may be thought of as the structure of Single - wall Carbon Nanotube. Two indices may be used to determine how the graphene sheet is folded (n, m). The numbers n and m denote the number of vector units between the two indicators in the graphene honeycomb's	Double-wall nanotubes are a crucial part of Multiwall carbon nanotubes. Although these materials have the same form as traditional Single wall carbon nanotube structures, they offer far better chemical resistance. This attribute is especially relevant if a cloning operation is necessary to add additional properties. Because Double-wall nanotube combines Single wall carbon nanotube and Multi wall carbon nanotubes transactions, it demonstrates the latter's electrical and thermal stability as well as the former's flexibility. The active Single wall carbon nanotube is at danger of being damaged since	It is represented as MWCNT. Several nested carbon nanotubes make up its structure. This particular sort of nanotube has two diameters, the outer diameter and the inner diameter.

	crystal structure. Nanotubes are referred to as zigzag nanotubes when m = 0, and armchair nanotubes when n = m. Otherwise, they're referred to as chiral. Given that the majority of their properties considerably alter at (n, m) values and that this dependence is non-monotonic, Single - wall Carbon Nanotubes are an important variation of carbon nanotubes.	it was built for a very specific use. The mechanical and electrical qualities of a structure can be altered by creating structural flaws. Double-wall nanotubes, on the other hand, just repairs the outside wall, keeping the inherent qualities. Double-wall nanotubes also has superior thermal and chemical stability than Single wall carbon nanotube, according to research. Technically crucial applications including gas sensors, dielectrics, nano composite materials, nano sensors, and field-emission displays can all benefit from Double-wall nanotube.	
Properties	(i)Diameter of SWCNT is around 2 nm (ii)Length of SWCNT is around 2 µm. (iii)Its Band gap varies from 0-2 eV. (iv)It shows metallic & semiconducting properties.	(i) This particular class of carbon nanotube consists of two nanotubes, with one nested within the other. (ii) Internal Diameter: 1-3 nm (iii) Outer Diameter: 2-4 nm (iv) Length: ~50µm	(i) It consists of several nested co-axial single wall CNT's. (ii) Inner Día: 1-3 nm (iii) Outer Dia: 2-20nm (iv) Length: 5-6µm

1.3 Carbon Nanotube Field Effect Transistor

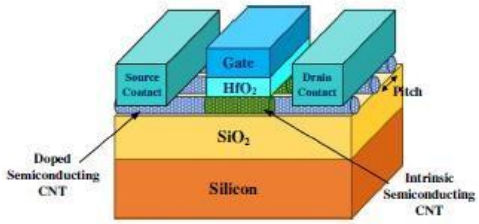


Figure 1 . Carbon Nanotube Field Effect Transistor (Prasad, Tayal, Yadav, Singla and Haseeb, 2019.)

The construction of Carbon Nanotubes Field Effect Transistor is shown above. The device is made up of silicon which forms the substrate of the device. A layer of silicon dioxide insulator is grown over the silicon substrate.

An Ideal Metal Oxide Semiconductor Field Effect Transistor like Carbon Nanotubes Field Effect Transistor is formed by one or more semiconducting Carbon Nanotubes perfectly aligned & well positioned whose part under the gate is Intrinsic and the source or drain extension areas are N-type/P-type doped depending on the kind of Carbon Nanotubes Field Effect Transistor.

As the source & drain regions are N-type doped & the channel is intrinsic, there is a potential barrier for the charge carriers from source to the drain region. This is the OFF state. Carrier (Electrons & Holes) do not see barrier in ON state.

Gate Electrostatic controls the top of the barrier similar to the conventional Metal Oxide Semiconductor Field Effect Transistor as shown in figure 1.

When positive voltage is applied to the gate, the barrier decreases & When the applied gate voltage exceeds the threshold voltage, a channel forms between the Source and Drain.

1.3.1 Applications of Carbon Nanotube Field Effect Transistor

i. Applied to solar cells.
ii. Mostly utilized in VLSI.
iii. Found in chips for quicker computers.

1.3.2 Advantages of Carbon Nanotube Field Effect Transistor

i. Low energy consumption.
ii. High Electro mobility.

iii. Reduced threshold voltages.

iv. Improved channel creation control.

v. The stream through the gate is lowered.

1.3.3 Disadvantages of Carbon Nanotube Field Effect Transistor

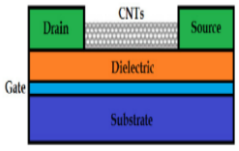
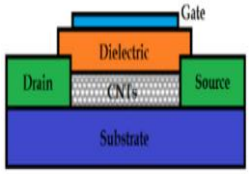
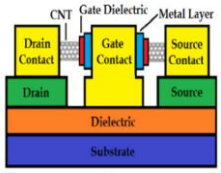
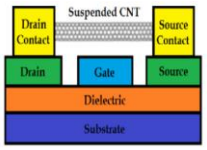
i. High temperature and strong electric current are not permitted.

ii. Complex Fabrication process

iii. High production cost

1.4 Types of Carbon Nanotube Field Effect Transistor

Table 2: Types of Carbon Nanotubes Field Effect Transistors (Bernal and Perez, 2012.)

Type	Back Gate	Top Gate	Wrap Around Gate	Suspended
Figure				
Description	In this process, a silicon dioxide layer is produced on top of the silicon layer during an earlier stage of manufacture. SiO_2 used as gate oxide layer to form the lithography bridge on Single layer	This structure built by high resolution electron beam lithography process in which carbon nano tubes are structured in pattern. Evaporation or atomic layer deposition are used to create a	Wrap around structure Carbon Nanotube are wrapped across the gate. This FET structure was first introduced in 2008. The complete nano tube is covered by a gate, which decreases leakage current and	The gate is hung above a trench in this manner to minimize the contact with oxides of gate & source with the result performance of the device improves. The disadvantage of this technology is that the gate electric is either air or vacuum. Because large tubes may come

	walled carbon nano tube to fabricated between the metal strips. These metal layer work as source & drain. To form the structure Carbon Nanotubes are positioned random along the metal strips. This type of model has low driving currents, low transconductance, and high parasitic contact resistance as its drawbacks. Next-generation Carbon Nanotubes Field Effect Transistor is created to get over these restrictions.	dielectric layer atop the carbon tube. Multiple top gate Carbon Nanotubes Field Effect Transistors may be built on a single wafer with electrically separated gates. The major advantage of this techniques is enhancement in drain current. Despite the fact that the fabrication process is complicated, this approach is chosen over the prior method.	enhances electrical performance. The production procedure begins with atomic layer deposition covering the carbon nano tube with a dielectric layer. The etching of the covering exposes the ends of the nanotubes.	into contact with the metal contact, shorting the device, only short Carbon Nanotubes are employed. It is not commercially available. It was utilized to study the inherent characteristics of clean Carbon Nanotubes.

1.5 Voltage - Current characteristics - Carbon Nanotubes Field Effect Transistor

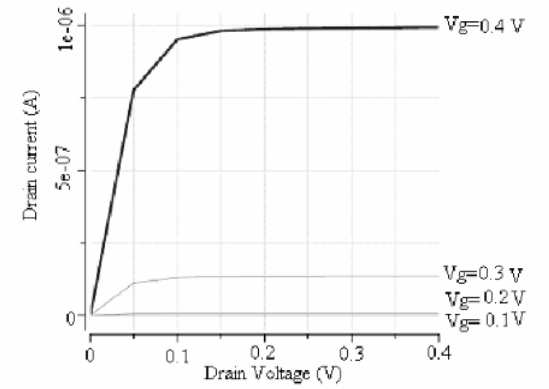


Figure 2. Voltage-current characteristics of Carbon Nanotubes Field Effect Transistor (Sahoo and Mishra, 2009)

To analyze the carbon nano tube field effect transistor for applied voltage at gate sources terminal keeping gate voltage constant it is observed that below the threshold voltage current produced at drain terminal is almost zero, but with increase in applied voltage as it reaches to the threshold limit the drain current start increasing gradually.

The current produced depends on barrier formed by the Schottky mechanism between drain and source. For fabricate the device contact silver, palladium, aluminum & titanium are most preferred metals.

1.6 Voltage Mode Circuits

Previously, every circuit utilized voltage mode topology or processed exclusively voltage signals. Let's look at a voltage power supply to help you understand voltage mode circuits. Voltage power supply must keep the output voltage constant regardless of the load current. which may range from 0 to the supply's maximum rated current, implying that the concern here is the voltage of the output terminals rather than the current. It is obvious that no circuit performs in an optimal manner in practise. Charge coupled devices and Switched capacitor circuits with performance similar to the necessary one are employed for this operation of delivering constant output voltage. According to the fundamental definition of voltage, it is the energy-to-charge ratio. Because the electron charges and the energy needed to transfer an electron from the valence band to the conduction band are both constants. For a

specific technology, voltage has an invariant value that provides a dependable voltage reference.

Advantages

i. Internal noise voltage created by noise currents help in determination of AC dynamic values for voltage mode circuits. The WB NSD is affected by device settings and biassing. The bandwidth and absolute frequency range have an impact on the total noise.
ii. Voltage measurement using various instruments and precise display is simple without causing any disruption to circuit elements. Despite having finite impedance, these circuits may easily drive compatible circuits with little effect on magnitude. As a result, these circuits are extremely important in both analog and digital circuit design.
iii. These circuits provide extremely effective cross regulation, and the reason for this is because they give low impedances at output terminals in the case of a supply with many outputs.
iv. These circuits employ a single feedback loop, making design and analysis simpler.

Disadvantages

When any kind of output modifications are noticed, a feedback loop is utilised for the purpose of correction, which slows down the circuit. To make up for the filter outputs that result in the inclusion of two poles in the control loop, the need of the dominant pole or a zero is added. Additionally, it complicates compensation since the loop gain changes in response to changes within the input.

1.7 Circuit Based on Current Mode

Historically, voltage signals dominated signal processing however, with the advent of submicron power technologies, the necessity for low power voltage supply has emerged.

However, employing voltage mode circuits to achieve this demand has limitations on linearity and dynamic range since it becomes challenging to build a circuit with excellent linearity and

dynamic range at submicron technology. Since the mentioned methods are relatively expensive, current mode processing has become a viable alternative during the past few decades. Low terminal impedence, which characterises current mode circuits and makes them appropriate for quick responses, Current mode circuits' output swing is increased when current is used as a signal, giving these circuits a better option for usage with low supply voltage. Therefore, current mode circuits have a greater dynamic range than voltage mode circuits for a given supply. These circuits are simpler than voltage mode circuits for purposes like addition and subtraction since they just need connecting the terminals at a single point to carry out these operations in current mode.

Advantages

i. Wide Bandwidth is one of the most important advantages of the current mode architecture.
ii. Power consumption is minimal even at high frequencies.
iii. It helps us to reduce the size of the feature.
iv. High Speed.
v. Some applications could need current mode interfaces, such the fiber-optic power measuring system, where the photodiode's input is required to be current.
vi. Controlled gain can be obtained without any elements in the feedback stream.
vii. Low Switching Noise and a wide dynamic range.

Disadvantages

i. High Distortion.
ii. High Gain variation.

Selection of circuit based on mode of application so as per the requirement volage or current mode circuit can be used.

2. LITERATURE REVIEW

Carbon nanotube & Carbon Nanotube based Field Effect Transistors circuit had been pre owned in digital circuit design. A great improvement in energy used and place effects to use of

Carbon Nanotube based Field Effect Transistors In different digital circuits, such as gates, adder, encoders, decoders, flip-flops, counters had already been designed by Carbon Nanotube based Field Effect Transistors.

Derycke, Martel, Appenzeller and Avouris (2001) this paper demonstrates possibilities of designing of field effect transistor by the Single wall Carbon nanotube. This transistor configuration is design with the help of doping and annealing technique.

The findings of paper shows inter and intermolecular design of inverter by Carbon nanotube field effect transistor. The result shows improved gain and electrical characteristics of inverter.

Pregaldiny, Kammerer and Lallement (2006) presented the case study of recent development in nano electrical devices. This work was present for bipolar and unipolar transistor configuration by Carbon nanotube field effect transistor. For design and analysis of proposed transistor configuration VHDLAMS modeling were used. This compact model of unipolar and bipolar Carbon nanotube field effect transistor validates transistor characteristic for unipolar and bipolar configuration.

Navi, Rastian, Khatir, Keshavarzian and Hashemipour (2010) demonstrated an inverter and three capacitors designed by CNTFET. Because it contains capacitors and inverters, this extra has a basic design. It is noticed that postponement and force defer items are created in the proposed structure. HSPICE programming was used to create the district.

Navi, Rad, Moaiyeri and Momeni (2010) designed and manufactured a full-length CNTFET cell-based cell with a variety of feeds, capacitive burden, and recurrence at a 32nm innovation hub. The HSPICE test system is used for reenactment at supply estimates of 0.5V and 0.65V. In comparison to its CMOS counterpart, the proposed configuration has improved speed and execution delay.

Ben-Jamaa, Mohanram and Micheli (2011) presented CNTFET-based flexile logic gates for ambipolar logic. Obtained the first standard NOR-NAND-AOI-OAI qualifications for operating XOR using CNTFETs. CNTFETs also design various blocks such as duplicates, straight circuits, and circuits. It has been observed that this significantly reduces material requirements, energy delays, and energy delay products in their structure.

Lin, Kim and Lombardi (2011) designed ternary logic gates based on CNTFETs. These logic gates are the result of power design and efficiency, and they offer alternatives to conventional concept gates. Imitation studies using SPICE simulation show that the ternary concept consumes less energy and requires fewer delays than traditional technology. According to SPICE abuse simulation research, the planned ternary concept consumes less energy and causes fewer delays than conventional technology. According to SPICE, the planned ternary logic consumes less power and has a shorter latency than standard technology.

Bagherizadeh and Eshghi (2011) created a dynamic full adder based on CNTFETs. It was discovered that, when compared to traditional Complementary metal oxide semiconductor (CMOS) technology-based adders, planned adders consume less power and have a shorter delay.

Kim, Kim and Choi (2011) presented new power gating strategies based on crossover innovation, such as when common point MOS and CNTFET are at 0.4V. Observations are proposed for gadget releasing power, surge current, and deferral are reduced by 69.07%, 5.96%, and 5.13%, respectively, when contrasted with its CMOS fundamentally based PG partner utilised in at 32nm technology.

Loan, Nizamuddin, Alamoud and Abbasi (2015) demonstrated analog blocks based on CNTFET. Significant advancements in operational transconductance amplifiers (OTAs) designed by CNTFETs were discovered.

Ansari and Tripathi (2017) created Current conveyor II (CC II) using CNTFETs on a 32 nm technology node. It was discovered that CC II based on CNTFET outperforms CMOS based CC II, i.e. conventional CC-II. The author worked on transient response, voltage transfer characteristics, current transfer characteristics, voltage and current gain, and voltage and current gain.

Laxya, Prasad, Mainuddin and Islam (2017) created a CNTFET-based voltage differencing transconductance amplifier (VDTA) that operated on the 32nm technology node and compared it to a conventional VDTA. He described the DC properties of VDTA and discovered that it performed better than conventional VDTA.

On the basis of CNTFET Prasad, Laxya, Mainuddin and Islam (2017) used the 32nm technology node for their current differencing buffered amplifier (CDBA), which compared CNTFET-CDBA to traditional CDBA. By describing the DC characteristics of CDBA, he achieved better results than traditional CDBA. The proposed circuit improves the input and output impedances at the W and Z terminals, respectively.

Zanjani, Dousti and Dolatshahi (2019) created a universal Gm-C filter based on CNTFETs with an inverter block made of OTA. Three inverters used in current-mode core circuit, this current-mode filter minimizes chip size and power consumption while functioning in all modes.
Laxya, Prasad, Mainuddin and Islam (2019) propose a Z-Copy current inverting transconductance amplifier (ZC-CITA) that is fundamentally based on CNTFET and its utility as a biquad channel and uses fewer additional substances, for example, by utilizing two capacitors with better transconductance, strength, and force utilization. This paper provides ZC-CITA, which is primarily dependent on CNTFET and provides a more general execution to analyze the CMOS structure. The final product has demonstrated the use of HSPICE for the technology node 32nm, input-yield characteristics, transconductance, and DC transfer characteristics. The circuit's enhancement is similarly demonstrated with a biquad clear out of 10k as the cut-off frequency.

Prasad, Tayal, Yadav, Singla and Haseeb (2019) present an operational transresistance amplifier based on CNTFETs (OTRA). OTRA has numerous advantages over traditional operational amplifiers. Some observations have also been made regarding how the number of CNTs of different CNTFET properties within the circuit influences the overall performance of the OTRA. Finally, the effects of optimising perceptions are observed. The outcomes are far superior to the traditional CMOS-based completely OTRA. Based on CNTFET- OTRA, an inverse pass filer is also designed.

Jogad, Afzal and Loan (2019) presented sinusoidal generator which designed by OTA as a fundamental structure. The utilization of CNTFET-OTA as application oscillator has completed the capacity advantages like tunable higher recurrence reach and temperature heartlessness when contrasted with conventional CMOS based OTA. The replicated outcomes have a commendable settlement with the hypothetical outcomes. As a result, the CNTFET-OTA quadrature oscillator has a far greater potential for developed wavering recurrence than the traditional CMOS-OTA fundamentally based oscillator.

Jogad, Afzal and Loan (2019) used HSPICE to plan and simulate CNTFET-Current Conveyor and CMOS-Current Conveyor at a 22-nm technology node innovation hub. The execution of CNTFET-CC attributes is regularly analysed by factoring in the various CNT boundaries. Examination reveals that CNTFET-CC has demonstrated significant improvements in voltage and current transmission capacity, higher impedance at port Y, less force dispersal, and lower THD when compared to standard CMOS-Current Conveyor. At 0.7V, a current mode obstruction to less dynamic channel circuits was recreated with filter reactions such as low pass, high pass, and band pass. It has been concluded from reactions that CNTFET-CC dynamic channels offer reactions going to ideal reactions with acquire solidarity. The most important aspect of the projected dynamic channel structure is the recognition of all channel capacities with fewer latent outer segments.

Jogad, Loan, Afzal and Alharbi (2020) have planned another 32 nm innovation for class AB - current conveyor II - based on carbon nanotube field effect transistor. This is related to the CMOS-based class AB - current conveyor II. The display of current conveyor II improves the distance and pitch of carbon nanotubes. The investigation discovered a remarkable improvement in boundaries such as current and voltage bandwidth across the terminal for protection. Normally, constant mutilation and normal energy are used in the evaluation of CMOS-based CC II current conveyors at 32 nm technology. This turnout also successfully examined the square/three-sided waveform generator designed by carbon nanotube field effect transistor CC II has better performance than CMOS-based CC II. This demonstrated square/three-sided waveform generator circuit is successfully recreated with successful execution in various boundary environments. It should be noted that this waveform generator outperforms existing technology, especially in low voltage, high slew rate, and low power consumption applications. It's a fantastic waveform generator structure created with the CNTFET CC II technique. Which strength in the oscillator circuit design.

In 2021, Akhoon, Alharbi, Bhat, Sunanda, Ashraf, and Loan developed and simulated an n-type carbon-nanotube field effect transistor-based current source load differential amplifier (CSL-DA). The suggested DA uses current source load and is built on CNTFETs with a 45nm technology node. The suggested CNTFET-based DA's performance has been contrasted with that of the more established MOSFET-based DA. In compared to the traditional DA, the suggested

DA has significantly improved across a number of key performance measurement criteria, according to the HSPICE simulation research. The special qualities of CNTs are responsible for the suggested device's improved performance. In comparison to its traditional MOS-based cousin, the CNTFET-based DA has been found to have a gain that is 2.7 times higher, a bandwidth increase of three orders, a gain bandwidth increase of 1180 times, and a power consumption decrease of almost 70%. The performance of the proposed DA can also be further optimized by adjusting various CNT parameters, including as the number of CNTs (N), CNT pitch (S), and CNT diameter.

Darwin, Rani, Raj, Appadurai and Balaji (2022) Carbon Nanotube Field Effect Transistors (CNTFETs) are good in the nano-material regime for giving improved performance in terms of power consumption despite device density. A CNTFET is a kind of FET in which the channel material is a single carbon nanotube (CNT) or arrays of carbon nanotubes rather than bulk silicon as in regular MOSFETs. There are other device architectures featured, such as double gate FETs and back gate FETs. Structure, functionality, and features of several types of CNTFETs have been discussed. Many aspects of CNTFETs have been studied, including their operation, dc parameters, and efficiency.

3. PROBLEM FORMULATION AND MOTIVATION

To share the information quickly and easily fast communication is the need of any system, this impacts the size and the power requirement of the hardware circuitry. This research work addressing both the issues of minimization of the size of the component and decrease the power requirements of the electronic device. Designing with the help of Carbon Nanotube reduces the power requirement, it also reduces the size of the electronic device.

4. OBJECTIVES OF THE STUDY

This research work is based on “Design and Analysis of Carbon Nanotube Based Analog Building Blocks and its Applications” has been taken with the following objectives.

i. To identify the existing techniques for design of Carbon Nanotube based Building Blocks.
ii. To reduce the size of device by optimizing the area and power consumption of existing designs.

iii. To evaluate the performance of designed Carbon Nanotube circuit block for voltage mode and current mode applications.

5. PROPOSED METHODOLOGY

Implementation of Carbon Nanotube with Analog Building Blocks using H-SPICE Software

5.1 HSpice

An analog circuit simulator called HSPICE can execute simulations in the transient, steady-state, and frequency domains. It is simple to convert existing SPICE decks for SPICE-3 to function with HSPICE, or to rebuild them to make use of features not included in SPICE-3. Since HSPICE is a commercial product with better support, it has higher convergence than SPICE-3. Additionally, it contains MetaWaves for interactive waveform viewing of input/output, hierarchical node naming, optimization of circuit and behavioral algebraic of parameterized cells. Hspice is extensively used in industry these days because it provides excellent numerical convergence, supports the newest device and connection models, and includes a huge variety of features for testing and improving circuits.

5.2 HSpice features

i. Excellent convergence.
ii. Extensive modeling accuracy, including foundry models.
iii. Naming and referencing of Node in hierarchy.
iv. Incremental and simultaneous optimization of model and cell circuit for AC, DC and transient simulation Multiparameter optimizations.
v. Tools for characterization of conventional cell libraries.
vi. Design of transmission lines for PCB, multichip, packaging, and IC technologies.

6. EXPECTED OUTCOME OF THE RESEARCH

CNTs have many applications and development of CNTFET is one of its important applications. CNTFETs have been used in the design and development of several analog circuits. The performance of these CNTFET-based analog circuits will compared to that of traditional CMOS-based circuitry. It has been generally observed that most of the

performance measuring parameters have improved significantly in the CNTFET based circuitry.

We will try to tap the advantages of CNTFETs by designing some existing analog building blocks employing n and p type CNTFETs to be simulated on H-Spice at 32nm technology node. The performance parameter such as power consumption, speed, current driving capability and the area of circuit optimization will be calculated using CNTFET technology. CNTFET is used to achieve the threshold voltage and to avoid large power dissipation. From this work CNTFET based structures of waveform generator would be design and simulate by H-spice Simulation Platform. The CNTFET based waveform generator would be compare with the conventional CMOS based waveform generator. Further, we will design 32 nm technology node based novel structure of CNTFET and CMOS based waveform generator, along with their applications.

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